In the Claims:

1. (Original) A method of forming a metal layer in an integrated circuit device, the method comprising:

forming a recess in a surface of an insulating layer, the recess having a side wall inside the recess, a bottom inside the recess, and an edge at a boundary of the surface of the insulating layer and the side wall;

forming a selective electroplating mask on the side wall to provide a covered portion of the side wall and to provide an exposed portion of the side wall that is free of the selective electroplating mask; and

electroplating a metal on the exposed portion of the side wall.

2. (Original) A method according to Claim 1 wherein forming a selective electroplating mask comprises forming the selective electroplating mask on the surface adjacent to the edge and on the side wall adjacent to the edge and not on the side wall beyond adjacent to the edge.

3. (Original) A method according to Claim 1 wherein electroplating comprises electroplating the metal on the exposed portion of the side wall and on the bottom to fill the recess with the metal to beneath a level of the electroplating mask on the side wall.

4. (Original) A method according to Claim 1 wherein forming a recess further comprises forming the recess to a depth that is about at least three times as great as a width of the recess.

5. (Original) A method according to Claim 4 wherein the width is in a range between about 0.05 μm and about 0.7 μm and the depth is in a range between about 0.2 μm and about 5 μm.

6. (Original) A method according to Claim 4 wherein forming a selective electroplating mask comprises forming an oxide layer on the insulating layer and the recess using sputtering or reactive vapor deposition.

7. (Original) A method according to Claim 6 wherein forming an oxide layer comprises forming the oxide layer to a thickness in a range between about 10 Ångstroms and about 500 Ångstroms.

8. (Original) A method according to Claim 4 wherein the insulating layer comprises a first insulating layer, wherein forming a selective electroplating mask comprises forming a second insulating layer on the first insulating layer and on the recess using plasma enhanced chemical vapor deposition.

9. (Original) A method according to Claim 4 wherein forming a selective electroplating mask comprises:

forming a metal layer on the first insulating layer and on the recess; and

oxidizing the metal layer.

10. (Original) A method according to Claim 1 wherein forming a recess is followed by:

forming a trench in the surface of the insulating layer on the recess that is wider than the recess, wherein the trench exposes the edge of the recess.

11. (Original) A method according to Claim 1 wherein the metal comprises a first metal, the method further comprising:

forming a second metal on the first metal.

12. (Original) A method according to Claim 1 wherein the metal comprises copper.

13. (Original) A method according to Claim 1 further comprising:

avoiding forming the selective electroplating mask on the covered portion of the side wall.

Claims 14-33 (Canceled).

34. (Original) A method for fabricating a metal layer in a semiconductor device, the method comprising:

forming an insulating layer having a concave portion on a semiconductor substrate;

forming a selective electroplating mask for exposing a portion of the conductive underlying layer, which is formed at an inside portion of the hole, and for covering at least a portion of the conductive underlying layer, which is formed at the edges of the mouth of the hole; and

selectively electroplating the inside of the concave portion that is exposed by the selective electroplating mask.

35. (Original) The method of claim 34, wherein the selective electroplating mask is formed of an insulating material.

36. (Original) The method of claim 35, wherein the selective electroplating mask is formed of a nitride or oxide made of aluminum, silicon, tantalum or titanium.

37. (Original) The method of claim 34, wherein forming the selective electroplating mask comprises:

forming a thin layer with aluminum, tantalum or titanium; and

oxidizing the thin layer.

38. (Original) The method of claim 34, wherein the metal layer is formed of copper (Cu), platinum (Pt), palladium (Pd) or nickel (Ni).

39. (Original) The method of claim 34 further comprises forming a seed layer, which is used for electroplating the metal layer, below the metal layer.

40. (Original) The method of claim 39, wherein the seed layer is formed of copper (Cu), tungsten (W), platinum (Pt) or gold (Au).

41. (Original) The method of claim 34, wherein a barrier metal layer is formed below the metal layer.

Claims 42-59(Canceled).

60. (Original) A method of forming a metal layer in an integrated circuit device, the method comprising:

forming a recess in a surface of an insulating layer, the recess having a side wall inside the recess, a bottom inside the recess, and an edge at a boundary of the surface of the insulating layer and the side wall;

forming a selective deposition mask on the side wall to provide a covered portion of the side wall and to provide an exposed portion of the side wall that is free of the selective deposition mask; and

depositing a metal on the exposed portion of the side wall.

61. (Original) A method according to Claim 60 wherein the depositing comprises sputtering the metal on the exposed portion of the side wall.

62. (Original) A method according to Claim 60 wherein the depositing comprises electroplating the metal on the exposed portion of the side wall.